UNIVERSITY OF JAMMU
NOTIFICATION
(10/April/ ADP/07)

It is hereby notified for the information of all concerned that the Vice-Chancellor in anticipation approval of the Academic Council, is pleased to authorize adoption of the revised Syllabi and Courses of Study in the subject of Electronics for B.Sc. Part-I of Three Year (General) Degree Course and M.Sc. I-Semester of Master's Degree Programme for the examination to be held in the year mentioned below alongwith the %age of change:-

B.Sc.	**Part-I**	**2011, 2012 & 2013**	**less than 10% in paper A & B**
M. Sc.	**Ist Semester**	**For the year Dec. 2010, 2011& 2012**	

Course No.	Course Title	%age of change
405	Electronics Devices & Circuits (EDC)	Less than 20%
406	Digital Electronics (DE)	Less than 20%
407	Physics of Semiconductor Devices (PSD)	Less than 20%
408	Computational Methods in Electronics (CME)	Less than 20%

Laboratory Courses

Course No. 418	Lab. Course in Electronic Devices & Circuits (Lab-I)	Less than 20%
Course No. 419	Lab. Course in Digital Electronic (Lab-II)	Less than 20%

F.Acd./Electronics/10/ 3878–3907
Dated: 27-04-2010

Sd/-
(DR. P.S. PATHANIA)
REGISTRAR

DETAILED SYLLABUS

B. Sc. Part-I

Subject: Electronics
Paper: A
Title: *Electronic Circuit Analysis*
Validity: Examinations to be held in 2011, 2012, and 2013

Duration of Examination: 3 Hrs
Max. Marks: 40

UNIT I. *Electronic components*

Resistors: fixed resistors (wire wound, film, and composite), variable resistors (mechanically & thermally variable), photo, and magneto; capacitors: specifications, fixed capacitors (vacuum, gas filled, foil, film, oil, mica, ceramic, and electrolytic), variable capacitors (mechanically & voltage variable); inductors: specifications and fixed inductors (air iron and ferrite cored); transformers: types, operation, IV relations, core types; autotransformer; transformer losses.

UNIT II. *Network analysis*

Kirchoff's laws, voltage and current sources; source transformations; mesh and nodal analysis; star delta transformations; network theorems: Thevenin's, Norton's, superposition, Millman, maximum power, and compensation.

UNIT III *A.C. circuit analysis*

Fundamentals: sinusoids, exponential functions, solution (exponential function, real and imaginary parts); resonance: series and parallel resonance (BW, resonance condition, impedance variation, effect of resistance, and reactance curves); coupled circuits: mutual inductance, coefficient of coupling, ideal transformer, series connection of coupled circuit.

UNIT IV *Analysis of R, L, C circuits*

Transient analysis of RC, RL, RLC circuits using differential equations; Laplace transform: transforms of linear combinations, transforms of derivatives & integrals, solution of problems using Laplace transform (partial fraction expansion and heavy side expansion theorem); solution of series RL, RC and RLC circuits using Laplace transform.

UNIT V *Filters*

Fundamentals: neper, decibel, current & voltage ratios as exponentials; symmetrical networks: properties, propagation, and Z_o; filter fundamentals: pass and stop bands, behavior of characteristic impedence, constant k low pass and high filters, m-derived T and pi section filters;

DETAILED SYLLABUS

B. Sc. Part-I

Subject: Electronics
Paper: B
Title: *Electronic Devices & Circuits*
Validity: Examinations to be held in 2011, 2012, and 2013

Duration of Examination: 3 Hrs
Max. Marks: 40

UNIT I. *Semiconductor diodes*

PN-junction diode: static and dynamic resistances, equivalent circuits, transition and diffusion capacitances; diode load line analysis; rectifier's analysis: half wave, full wave, and bridge; clippers and clampers; Zener diode and its applications; Schottky diode: construction, working, and characteristics; special diodes: LED, Solar cell, Photo, Tunnel, and Varactor diode.

UNIT II *Transistors*

BJT: biasing: fixed bias, collector feedback, and voltage divider; stabilization and bias compensation; FET: construction and characteristics, Schokley equation, transfer curve, biasing (self and voltage divider); construction, working, and characteristics of MOSFET, Phototransistor; and UJT.

UNIT III *Amplifiers*

h-parameters and equivalent circuit; BJT small signal analysis for CE, CB, and CC: input impedence, current and voltage gains, and output impedance; cascading: RC coupled, TC, and DC amplifiers (circuit, analysis, and frequency response); Power amplifiers: class A, B, and C; class-B Push-pull amplifier.

UNIT IV *Feedback and oscillator circuits*

Analysis of voltage series, voltage shunt, current series, and current shunt feedback configurations; effect of negative feedback; simple practical feedback circuits; Barkhausen criterion; analysis of phase shift, Wein bridge, Hartley, Colpitt's, Clapp's, and crystal oscillators.

UNIT V *Integrated circuits*

Integrated circuits: advantages, disadvantages, integration scales; classifications of ICs; Czochralski technique of crystal growth; fabrication of monolithic ICs: vapor phase epitaxy, photo-lithographic techniques for doped and un-doped layers, masking, [illegible] diffusion and

DETAILED SYLLABUS

M. Sc. ELECTRONICS 1st SEMESTER

Course No: 405
Title: *Electronic Devices & Circuits* (EDC)
Credits: 4
Validity: 2010, 2011, and 2012 December exams

Duration of Examination: 3 Hrs
Max. Marks: 100
Semester Exam: 80
Sessional Assessment: 20

UNIT I. *Electronic Devices and Applications*

Transistor Biasing and Stabilization with design problems, h-parameters and their applications in transistor circuit analysis for CE, CB and CC configurations; FET and MOSFETs: Characteristics and Biasing, Design of biasing circuits, Design and analysis of amplifiers, Numerical problems.

UNIT II. *Frequency response of amplifiers*

General concepts; bode plot; low frequency response: BJT and FET amplifiers; miller effect capacitance; high frequency response of BJT amplifiers; hybrid pie model: short circuit current gain, cut off frequency, and current gain with resistive load; high frequency response of FET amplifiers; frequency response of multistage amplifiers; square wave testing, Numerical problems.

UNIT III. *Analysis of compound configurations*

Cascade connection; Cascode connection; Darlington connection; Bootstrapping principle; Bootstrapped Emitter Follower; Bootstrapped Darlington Emitter Follower; Feedback pair; CMOS circuits; Current source circuits; Current mirror circuits; Differential amplifier circuits; Numerical problems.

UNIT IV. *Power amplifiers*

Introduction, Series-fed Class A amplifier, Transformer coupled class A amplifier, Class B amplifier operation, Class B amplifier, Amplifier distortion, Power transistor heat sinking, Class C and Class D amplifiers, Numerical problems.

UNIT V. *Power supplies and voltage regulators*

References:

1. L. Boylestad and Louis Nashelsky, **Electronic devices and circuit theory**, Prentice-Hall of India, New Delhi.
2. Millman and Halkias, **Integrated electronics**, Tata McGraw-Hill, New Delhi.
3. Mottershed, **Electronic devices and circuits**, Prentice-Hall of India, New Delhi.
4. M. S. Ghausi, **Electronic devices and circuits**, CBS.
5. Donald L. Schilling and Belove, **Electronic circuits**, Tata McGraw-Hill, New Delhi.
6. Millman and Grabel, **Microelectronics**, Tata McGraw-Hill, New Delhi.
7. Bogart, **Electronic devices and circuits,** Universal Book Stall, New Delhi.
8. Mark N. Horenstein, **Microelectronic circuits and devices**, Prentice-Hall of India, New Delhi.

DETAILED SYLLABUS

M. Sc. ELECTRONICS 1st SEMESTER

Course No: 406
Title: *Digital Electronics* (*DE*)
Credits: 4
Validity: 2010, 2011, and 2012 December Exams

Duration of Examination: 3 Hrs
Max. Marks: 100
Semester Exam: 80
Sessional Assessment: 20

UNIT I. *Combinational logic design*
Canonical and Standard forms, Karanaugh Map: SOP & POS minimization, Five variable K-maps; Binary Adder, Carry lookahead Adder, 4-bit Adder-Subtractor, BCD Adder, Binary Multiplier, Comparator, Decoder, Encoder, Multiplexer, Demultiplexer.

UNIT II. *Sequential system design*
Review of Flip-flop; Mealy & Moore Models; Analysis of Synchronous Sequential Circuits; Construction of State Diagrams: Up/Down Decade Counter, Sequence Detectors, Serial Ex-3 to BCD Code Converter; Counter Design: Modulo-8 & Up or Down Decade Counter; State Equivalence; State Reduction, State Assignment Techniques.

UNIT III. *Memory and Programmable Logic*
General Memory Operation; CPU-Memory Connections; ROM: Architecture, Timing, Types: MROM PROM, EPROM, EEPROM, Flash Memory; RAM: Architecture & Operation of SRAM, DRAM; Memory Expansion; Introduction to Programmable Logic Devices (PLDs): PLA, PAL, GAL, CPLD, FPGA.

UNIT IV. *Computer Architecture-I*
Instruction Codes; Computer Registers; Instructions; Timing and Control; Instruction Cycle; Register and Memory Reference Instructions; Design of Basic Computer: Control of Registers, Memory and Common Bus; Design of Accumulator Logic; Microprogrammed Control: Control Memory, Address Sequencing: Conditional Branching, Mapping of Instruction, Microinstructions, Microoperation, Microprogram; Design of Control Unit, Microprogram Sequencer.

UNIT V. *Computer Architecture-II*

References:

1. T. L. Floyd & R. P. Jain, **Digital fundamentals,** Pearson Education India, New Delhi.
2. M. Moris Mano, **Digital Design,** PHI Learning Pvt. Ltd. New Delhi.
3. A. P. Malvino & D. P. Leach, **Digital Principals and Applications**, Tata McGraw Hill, New Delhi.
4. A. P. Malvino & J. A. Brown, **Digital Computer Electronics**, Tata McGraw Hill, New Delhi.
5. A. Anand Kumar, **Fundamentals of Digital Circuits,** PHI Pvt. Ltd. New Delhi.
6. R. J. Tocci & N. S. Widmer, **Digital Systems**, Pearson Education India, New Delhi.
7. John. M. Yarbough, **Digital Logic: Applications and Design**, Thomson Brooks/Cole, Boston.
8. John F. Wakerly, **Digital Design Principles and Practices**, Pearson Education India, New Delhi.
9. M. Moris Mano, **Computer System Architecture**, PHI Pvt. Ltd. New Delhi.

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DETAILED SYLLABUS

M. Sc. Electronics Ist Semester

Course No: 407
Title: **Physics of Semiconductor Devices (PSD)**
Credits: 4
For the years: 2010, 2011 & 2012

Duration of Examination: 3hrs
Max. Marks: 100
Semester Exam: 80
Sessional Assessment: 20

UNIT I **Carrier Concentration & Transport**

Introduction to Electronic Materials, Crystal Structures of Si and GaAs, Miller Indices, band theory of solids, Fermi levels in intrinsic and doped semiconductors, degenerate semiconductors derivation of intrinsic carrier concentration, carrier mobility and drift velocity, resistivity and conductivity, Hall effect, diffusion phenomenon, Haynes-Shockley experiment, Einstein's relationship, carrier injection & recombination processes, Auger recombination, continuity equation, high field effects.

UNIT II **P-N Junction Theory**

P-N junction: thermal equilibrium condition, depletion region (abrupt and linearly graded junctions), depletion capacitance: C-V characteristics, impurity distribution, and varactor; I-V characteristics; generation-recombination and high-injection effects, temperature effect, charge storage and transient behaviour; minority carrier storage, diffusion capacitance, junction breakdown: tunneling effect and avalanche multiplication; semiconductor heterojunctions.

UNIT III **BJT's and MESFET's**

The Transistor action, active mode operation, current gain, Static characteristics,; modes of operation (Ebers-Moll Model), I-V characteristics of CB and CE configurations, frequency response and switching transients; basic concepts of HBT, basic concepts of thyristors.

Metal-semiconductor contacts: Schottky barrier and Ohmic contacts (energy band relation), C-V characteristics; MESFETs(Normally-Off/On): structure, operation, I-V characteristics and high frequency performance; MODFET: structure and I-V characteristics.

UNIT IV **Theory of MOS Devices**

Ideal MOS diode; surface depletion region and ideal MOS curves; Sio_2 – Si MOS diode: interface traps and oxide charges; drain current derivation, The MOSFET: basic characteristics and types, threshold voltage and device scaling: short channel effects, drain induced barrier lowering, and scaling rules; CMOS and BiCMOS: CMOS inverter, and TFT.

UNIT V **Photonic/Microwave Devices**

Energy momentum relationship, direct and indirect band semiconductors transferred electron effect, quantum mechanical tunneling, Hot electron effect; emission in semiconductors, optical absorption,

DETAILED SYLLABUS

M. Sc. ELECTRONICS 1st SEMESTER

Course No: 408
Title: *Computational Methods in Electronics* (CME)
Credits: 4
Validity: 2010, 2011, and 2012 December exams

Duration of Examination: 3 Hrs
Max. Marks: 100
Semester Exam: 80
Sessional Assessment: 20

UNIT I. *Complex variables*

Review of complex algebra; functions of a complex variable; Cauchy- Riemann equations; Cauchy integral theorem; Cauchy integral formula, Taylor's and Laurent's series; Cauchy residual theorem; applications to contour integration; singular points and evaluation of residues; definite integrals; Jordan's lemma; mapping translation; rotation; inversion and conformal mapping; problems.

UNIT II. *Series solution of Differential Equations*

Lengendres differential equation; generating function of Pn(x); recurrence relation for Pn(x); Rodregnes formula; associated legendres polynomial; Bessel's differential equation; generating function for $J_n(x)$ and their recurrence relations;

UNIT III. *Numerical Methods-I*

Errors: sources, propagation and analysis; Solution of non linear equations: Bisection, Newton-Raphson and secant method; Interpolation and polynomial approximation: Lagrange and Newton polynomials and approximation; Splines; numerical solutions of differential equations: Euler's method, Taylors series method and Runga-Kutta method (IInd Order).

UNIT IV. *Numerical Methods-II*

Solution of system of linear equations: Gauss elimination, Pivoting, LU-factorization, Gauss Jordan method; Gauss-Seidal iteration method, Jacobi iteration, Ill conditioning, Norms, Method of least squares, Matrix eigen value problems, Inclusion of matrix eigen values, Eigen values by iteration (Power method).

UNIT V. *Probability and Statistics*

References:

1. John Methew, **Numerical methods for mathematics science and engineering**, Prentice-Hall of India, New Delhi.
2. Kendall E Alkinson, **An introduction to numerical analysis**, John Willey and Sons, New York.
3. E. Kryszig, **Advanced engineering mathematics.**
4. Mary L. Boas, **Mathematical methods in physical Sciences**, Wiley International.
5. C. Harley Harps, **Intoduction to mathematical physics**, Prentice-Hall of India, New Delhi.
6. V. Rajaraman, **Computer oriented numerical methods**, Prentice-Hall of India, New Delhi.
7. M.K. Jain, S.R.K. Iyengar and R.K. Jain, **Numerical Methods: Problems and Solutions**, New Age International, New Delhi.

DETAILED SYLLABUS

M. Sc. ELECTRONICS 1st SEMESTER

Course No: 418
Title: Lab course in Electronic Devices & Circuits (Lab-I)
Credits: 4
Validity: 2010, 2011 and 2012 December Exams.
Duration of Examination: 6 Hrs

Max. Marks: 100
Semester Exam: 50
Sessional Assessment: 50

Each student has to perform a total of ten experiments including the mini project, which is mandatory. The teacher incharge may add or delete experiments as per the availability of the equipment and need of the course with the authorization of the Head of the Department.

List of Experiments

1. Familiarity, testing and fault detection of electronic components and tools.
2. PCB design.
3. Transformer design.
4. Calculation of barrier height and ideality factor at room temperature (for Si and GaAs devices) from the *I-V* characteristics.
5. Calculation of diode parameters at varying frequency from the *C-V* characteristics.
6. Calculation of semiconductor conductivity type and carrier concentration using Hall Effect.
7. Calculation of semiconductor resistivity and band gap using Four-Probe method.
8. Calculation of carrier mobility and drift velocity using an experimental setup.
9. Study of transistor biasing circuits (BJT, FET, MOSFET).

DETAILED SYLLABUS

M. Sc. ELECTRONICS 1st SEMESTER

Course No: 419
Title: Lab course in Digital Electronics (Lab-II)
Credits: 4
Validity: 2010, 2011 and 2012 December exams
Duration of Examination: 6 Hrs

Max. Marks: 100
Semester Exam: 50
Sessional Assessment: 50

Each student has to perform a total of ten experiments including the mini project, which is mandatory. The teacher incharge may add or delete experiments as per the availability of the equipment and need of the course with the authorization of the Head of the Department.

List of Experiments

1. Design of Adder/Subtractor.
2. Design of Comparator.
3. Design of Multiplexer/Demultiplexers.
4. Design of Flip-Flops.
5. Design of Counters.
6. Design of Registers.
7. Design of Encoders.
8. Design of Decoders.
9. Design of finite state machine